In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Currently Amended) A Booth encoding circuit comprising:

a plurality of cells, wherein at least one of said cells comprises:

a plurality of inputs;

a first plurality of transistors forming a ~~first~~ NAND logic stage, wherein at least one of said inputs is connected to at least one of said first plurality of transistors;

a second plurality of transistors forming ~~a second~~ an OR logic stage, wherein at least one of said inputs is connected to at least one of said second plurality of transistors;

a first output inverter connected to at least one of said second plurality of transistors;

a first switching means connected to at least one of said first plurality of transistors;

a second switching means connected to said first output inverter;

a second output inverter connected to said first switching means and said second switching means, wherein within a critical path of said Booth encoding circuit said first output inverter drives said second output inverter.

2. (Original) The Booth encoding circuit of claim 1, wherein within said critical path of said Booth encoding circuit said first output inverter drives said second output inverter via said second switching means.

3. (Original) The Booth encoding circuit of claim 2, wherein said first switching means comprises a first transfer gate switch

and said second switching means comprise a second transfer gate switch.

4. (Canceled)

5. (Currently Amended) The Booth encoding circuit of claim ~~4~~ 1, wherein said critical path comprises at least two of said second transistors, said first output inverter, said second switching means, and said second output inverter.

6. (Original) The Booth encoding circuit of claim 5, wherein a critical path transistor level within said cell is less than six and a critical path transistor level within said Booth encoding circuit is less than ten.

7. (Currently Amended) The Booth encoding circuit of claim ~~4~~ 1, wherein an output of said second output inverter is logically expressed by the formula $Y_{2n+1} * (Y_{2n} * Y_{2n-1}) + Y_{2n+1} * (Y_{2n} + Y_{2n-1})$, wherein said plurality of inputs comprise Y_{2n}, Y_{2n-1}, and Y_{2n+1}.

8. (Original) The Booth encoder of claim 2, wherein said cell further comprises an input inverter connected to said first switching means and at least one of said inputs.

9. (Original) The Booth encoder of claim 8, wherein at least one of said inputs is connected to said second switching means.

10. (Currently Amended) A multiplier comprising:

A Booth encoding circuit, wherein said Booth encoding circuit comprises a plurality of cells, wherein at least one of said cells comprises:

a plurality of inputs;

a first plurality of transistors forming a ~~first~~ NAND logic stage, wherein at least one of said inputs is connected to at least one of said first plurality of transistors;

a second plurality of transistors forming ~~a second~~ an OR logic stage, wherein at least one of said inputs is connected to at least one of said second plurality of transistors;

a first output inverter connected to at least one of said second plurality of transistors;

a first switching means connected to at least one of said first plurality of transistors;

a second switching means connected to said first output inverter;

a second output inverter connected to said first switching means and said second switching means, wherein within a critical path of said Booth encoding circuit said first output inverter drives said second output inverter.

11. (Original) The multiplier of claim 10, wherein within said critical path of said Booth encoding circuit said first output inverter drives said second output inverter via said second switching means.

12. (Original) The multiplier of claim 11, wherein said first switching means comprises a first transfer gate switch and said second switching means comprise a second transfer gate switch.

13. (Canceled)

14. (Currently Amended) The multiplier of claim ~~13~~ 10, wherein said critical path comprises at least two of said second transistors, said first output inverter, said second switching means, and said second output inverter.

15. (Original) The multiplier of claim 14, wherein a critical path transistor level within said cell is less than six and a critical path transistor level within said Booth encoding circuit is less than ten.

16. (Currently Amended) The multiplier of claim ~~13~~ 10, wherein an output of said second output inverter is logically expressed by the formula $Y_{2n+1} * (Y_{2n} * Y_{2n-1}) + Y_{2n+1} * (Y_{2n} + Y_{2n-1})$, wherein said plurality of inputs comprise Y_{2n}, Y_{2n-1}, and Y_{2n+1}.

17. (Original) The Booth encoder of claim 11, wherein said cell further comprises an input inverter connected to said first switching means and at least one of said inputs.

18. (Original) The Booth encoder of claim 17, wherein at least one of said inputs is connected to said second switching means.

19. (Currently Amended) A multiply-accumulate module comprising:

a multiplier, wherein said multiplier comprises:

A Booth encoding circuit, wherein said Booth encoding circuit comprises a plurality of cells, wherein at least one of said cells comprises:

a plurality of inputs;

a first plurality of transistors forming a ~~first~~ NAND logic stage, wherein at least one of said inputs is connected to at least one of said first plurality of transistors;

a second plurality of transistors forming ~~a second~~ an OR logic stage, wherein at least one of said inputs is connected to at least one of said second plurality of transistors;

a first output inverter connected to at least one of said second plurality of transistors;

a first switching means connected to at least one of said first plurality of transistors;

a second switching means connected to said first output inverter;

a second output inverter connected to said first switching means and said second switching means, wherein within a critical path of said Booth encoding circuit said first output inverter drives said second output inverter.

20. (Original) The multiply-accumulate module of claim 19, wherein a critical path transistor level within said cell is less than six and a critical path transistor level within said Booth encoding circuit is less than ten.